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Frequency Scaling Based Power Efficient Flip-Flop Design in 28nm FPGA

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ABSTRACT: The developing business sector of portables like mobile phones, gaming consoles and battery controlled electronic frameworks need to limit power utilization. It is continuously demanding to design devices which have low power consumption. Most VLSI circuits are sequential. Elementary building blocks of sequential circuits are flip-flops which are used to store information for any digital electronic and control circuit. In this paper, power efficient SR and D flip flops have been designed using the Artix 7 family in FPGA. The power dissipation is reduced using frequency scaling technique. The design tool used is Xilinx 14.2 ISE and the RTL logic of the flip flops has been designed using Verilog coding. The ambient temperature of 25°C is utilized to design low power SR and D flip-flop circuits. The frequency has been scaled from 1GHz to 8GHz for both SR and D flip flops. Hence the frequency scaling technique in SR flip-flop is able to reduce the total power consumption from 13.4% to 1.17% at a junction temperature of 25.4°. On the other hand the frequency scaling technique in D flip-flop is able to reduce the total power consumption from 12.5% to 1.19% at a junction temperature of 25.4°.

Keywords: Artix 7, Field Programmable Gate Arrays (FPGA), Frequency Scaling, Low Power Flip Flop Design, Power Dissipation, Xilinx.

Abbreviations: CMOS, Complementary metal oxide semiconductor; FPFA, Field programmable gate array; SR Flip Flop, Set – Reset Flip flop, D Flip Flop, Delay Flip flop; RTL, Resistor transistor logic; VLSI, Very large Scale Integration.

I. INTRODUCTION

Any superior circuit requires an enormous number of transistors with fast speed. For this enhancement in performance, power dissipation comes along. High package density is a major requirement of VLSI technology, as the physical dimensions of the transistor get more compact with time [1]. As indicated by Moore's law, the number of transistors on a microchip doubles every two years, as the cost of computers is getting halved. Moore's Law justifies that one can predict the speed and capability of one's PCs to enlarge each couple of years, and one can retain more money on them. Another proposition of Moore's Law also affirms that this technological evolution is rampant. Today, notwithstanding, the multiplying of introduced transistors on silicon chips happens nearer to every 18 months rather than every two years [2].

As per today's larger technological demands, total power dissipation is increasing remarkably. The power dissipation escalates cooling costs as well as decreases reliability of the system. Supposedly, there are two principle origins of power dissipation in every processor i.e Static power dissipation and dynamic power dissipation. The main reason for static power dissipation is leakage current. This leakage current is defined as the very small flowing current through a device or transistor when it is in inactive mode. The main reasons for dynamic power dissipation are switching transient current and short circuit power dissipated. Latest System-on-Chip requests larger power. Both in memory and logic, static power is expanding simultaneously with the rise in dynamic power. Therefore, total power is dramatically expanding. All the developing business areas of portable electronic equipment, for example, mobile phones, ultra-speed gaming consoles and each and every battery-controlled electronic frameworks needs microelectronic circuits which have very low power dissipation and low supply voltages. If every semiconductor integration keeps on observing Moore's Law, the power density in the electronic chips will reach way higher than the rocket spout [3]. CMOS downscaling operations have enforced continuous decline of operating supply voltages for analog circuits. The following trend has been reasonably driven by the demand of Very Large-Scale Integration (VLSI) systems in which it was necessary to ideally stop oxide breakdowns with declining gate-oxide thickness and to lower power consumption of any digital circuitry [4]. Most VLSI circuits are sequential. An intriguing observation shows that a logic set-up and a clock segment alone consumes the same power in varying microchips, in which the clock segment itself utilizes nearly 20%-45% of the total microchip power. Under this clock segment power, 90% is used by flip flops themselves and along with the furthest branches of the clock distribution network straight driven by the flip-flops [5].

II. LITERATURE REVIEW

The expanding prominence quality of compact systems and the need to limit power utilization is continuously demanding the designers to design the devices which use low power consumption. The flip-flop design make use of latest gating procedures which lessen power consumption by deactivating the clock signal.

Introduced circuits vanquish the clock obligation period confining recently detailed gated flip-flops. Circuit approximate imitation with the incorporation of parasitic shows that reasonable decrease power consumption is conceivable whenever information signal has diminished switching movement [6]. The power reduction can also be possible using twofold edge activated (DET), rather than ordinary single edge activated (SET) flip-flops. The examination incorporates an execution of autonomous investigation for the impact of the information successions in the energy consumption of single and twofold edge triggered flip-flops. The framework level vitality reserve funds conceivable by using registers consisting of double edge triggered flip-flop, instead of single edge triggered flip-flop, is in this manner investigated [7].

The researchers had created a strategy for choosing and advancing flip-flops for low-vitality frameworks with steady output. Portrayal measurements, pertinent low-vitality frameworks are talked about, giving information into timing and vitality boundaries at two of circuits and framework levels. Transistor parameters are upgraded for negligible delay under compelled energy utilization. A transference-gate master-slave latch pair has the biggest inside channel, most reduced energy dissipation, and has energy-postpone item tantamount to a lot of quicker pulse-triggered latches [8]. In a paper [9], SR and JK flip-flop structures reliant on the transmission-gate adiabatic rationale with NMOS pull-down arrangement are presented. In light of the re-enactment results, these adiabatic flip-flops beat their CMOS accomplices to the extent of power utilization. The movement of a 4- bit binary counter created utilizing the offered JK flip-flop has likewise recreated and affirmed. Some researchers also conveyed that a flip-flop circuit incorporates a differential Stage coupled to a straightforward latch. Particular edges of the differential Stage, insinuated as the “output Side” and the “reference Side,” are pre-charged high during a pre-charge phase. During the evaluation phase, the transparent latch is empowered and upon commencement of the following pre-charge stage, the see-through latch is rapidly disabled. Since just a Single side of the differential Stage is utilized to drive the see-through latch, the differential Stage may profitably be actualized in an asymmetric fashion. Likewise, during an evaluation phase, the condition of an information input Signal is detected. Contingent on the condition of the input Signal, either the output Side or the reference Side is released. All the more particularly, transistors framing the reference side of the differential Stage might be created utilizing littler channel widths than comparing transistors shaping the yield side of the differential Stage [10].

It beneficially permits fast usage of the flip-flop circuit while reducing lethargy, clasp-time, and power utilization. Natarajan [11] have presented the operations and timing diagrams of various flip flops and presented its fundamentals. Pooja *et al.*, [12], the flip flops have been designed using 45nm technology. The results proves that the overall occupational area and power consumption had been reduced. By Varying Voltage and frequency of a graphical processing unit, high performance system has been generated in paper [13]. Kiat *et al.*, [14] a processor has been reconfigured which results in high performance and low energy consumption. Ahmed [15] has introduced efficient FPGA based architecture using voltage scaling. The system is energy efficient. Fang *et al.*, [16] has surveys various FPGAs so that they can perform in comparison with the memory system. Lee *et al.*, [17] has designed the clocked flip flops at 28nm that can operate at the temperature range of -40 degree Celsius to 120 degree Celsius.

Sakthivel and Rai [18] has proposed a memristor based D flip flop in CMOS which has lower latency and power dissipation. Honnavara Prasad [19] had published a design of a processor circuit having low power consumption. Swamynathan and Bhanumathi [20] has designed FPGA based SRAM with lower energy consumption with higher stability. Hence the designs proposed using FPGA based platforms will have higher stability and lower power consumption. In this paper, frequency scaling of the basic memory unit i.e. flip flop is worked upon and power dissipation is examined accordingly.

III. PROPOSED DESIGNS

A. Proposed design of SR flip-flop

The SR flip-flop is reviewed as one of the most fundamental sequential logic circuit conceivable and which is also essentially a one-bit memory bistable device having two sources of info, one of which named as S will "SET" the device giving output as 1, and the other named as R, will "RESET" the device giving output as 0. RTL logic which stands for resistor transistor logic consists of resistor inputs and bipolar junction transistors as switching devices.

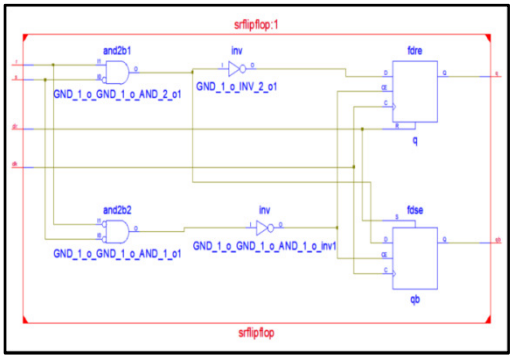

Fig. 1. Shows RTL logic of proposed SR flip-flop.

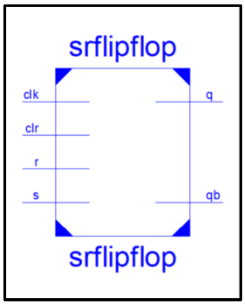

Fig. 2. Shows block diagram of proposed SR flip-flop.

Fig. 1 shows the RTL logic of SR flip flop contains two AND gates, two inverters and two bit storing registers. The characteristic equation of SR flip flop is Q (next) = S +R'Q (previous).
It is clear from Fig. 2 that SR flip-flop has two input signals- S and R, a clock signal as well as a clear signal. If at any time, clear signal becomes an active high it means the flip-flop will always give an output zero and if clear signal is active low or equals to zero, the values of SR and clock will decide the value of output q and hence the value of qb. The value of q is always low when clear signal is high. The rest values of the output q and qb depends on the truth Table of SR flip-flop which says whenever the clock triggers, if S and R are both zero, value of flip flop remains unchanged, if input S is high then output q is high and qb is low and if input R is high then output qb is high and q is low. The behavior is indeterminate if both values of S and R are 1.

B. Proposed of D flip-flop

Fig. 3 shows RTL logic of D flip flop. It keeps in check the input, by producing advances that coordinate that of the input D. Here, the alphabet D means "data". The D flip-flop retains the worth that is on the data line. A set/reset flip flop can be used to produce D flip-flop by binding the set and reset together through an inverter. A D flip-flop attempts to follow the input D however can't make the necessary changes except if it is empowered by the clock [12].
It is clear from Fig. 4 that D flip-flop has one input signal d, a clock signal and a clear signal as well. If at any time, the clear signal becomes an active high it means the output of flip-flop will always be a zero and if the clear signal is active low or equals to zero, the values of D and clock will decide the value of output y. The value of y is always low when clear signal is high. The rest values of the output y depends on the truth table of D flip-flop which says whenever the clock triggers, the flip flop acts as a delay unit, which means, if the D(input) is low, then y(output) becomes low and similarly if D is high, then y becomes high.

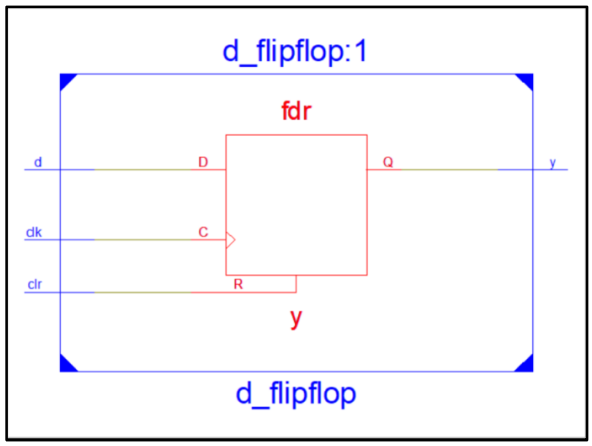

Fig. 3. RTL logic of proposed D flip-flop

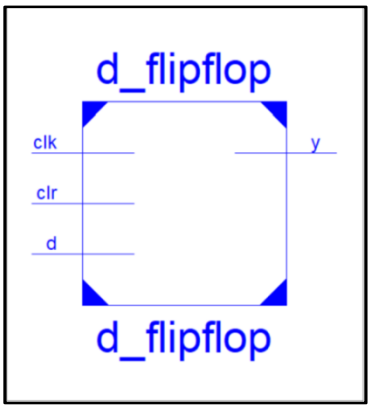

Fig. 4. Block diagram of proposed D flip-flop.

IV. RESULTS OF FREQUENCY SCALING

Frequency scaling is performed using the Artix7 family at junction temperature 25℃. It is productive to reduce power consumption. The SR and D flip flops are operated on a frequency range of 1GHz to 8GHz. Frequency scaling results are as per the following.

A. Frequency Scaling of SR Flip-Flop

When the SR flip-flop operates at 1V, the value of leakage current is 0.082 Watts at junction temperature of 25.4℃. Table 1 shows the total output power of SR flip flop at the frequency range from 1GHz to 8GHz. From the table, it is clear that the total power value in watts is reduced from 0.097 Watts to 0.084 Watts as the frequency increases from 1GHz to 8GHz. The maximum reduction of power dissipation is 13.4% at 1GHz. The minimum and maximum value of total power is at 8GHz and 1GHz respectively.

Table 1: Power Dissipation of SR Flip flop with Artix 7 FPGA at junction temperature of 25.4^{0}C.

Frequency(F) GHz	Leakage Power (L.P) watts	Total Power (T.P) watts
1	0.082	0.097
1.2	0.082	0.095
1.8	0.082	0.091
2	0.082	0.090
3	0.082	0.088
4	0.082	0.086
5	0.082	0.085
8	0.082	0.084

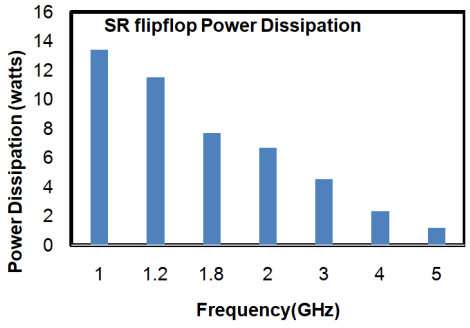

Fig. 5. Power dissipation and Frequency graph of SR Flip Flop.

Fig. 5 shows the graph between the frequency and power dissipation. It is concluded from the following graph that the frequency is increased from 1GHz to 8GHZ and with the increase in the frequency, the power dissipation is decreasing for SR flip-flop.

B. Frequency Scaling of D flip-Flop

When the D flip-flop operates at 1V, the value of leakage current is 0.082 Watts at junction temperature of 25.4℃.

Table 2 shows the total output power of D flip flop at the frequency range from 1GHz to 8GHz. From the table, it is clear that the total power value in watts is reduced from 0.096 Watts to 0.084 Watts as the frequency increases from 1GHz to 8GHz. The maximum reduction of power dissipation is 12.5% at 1GHz. The maximum and the minimum value of total power is at 1GHz and 8GHz respectively.

Table 2: Power Dissipation of D Flip flop with Artix 7 FPGA at junction temperature of 25.4^{0}C.

Frequency (F) GHz	Leakage Power (L.P) watts	Total Power (TP) watts
1	0.082	0.096
1.2	0.082	0.093
1.8	0.082	0.090
2	0.082	0.089
2.9	0.082	0.087
4	0.082	0.086
5	0.082	0.085
8	0.082	0.084

Fig. 6 shows the graph between the frequency and power dissipation. It is concluded from the following graph that the frequency is increased from 1GHz to 8GHZ and with the increase in the frequency, the power dissipation is decreasing for D flip-flop.

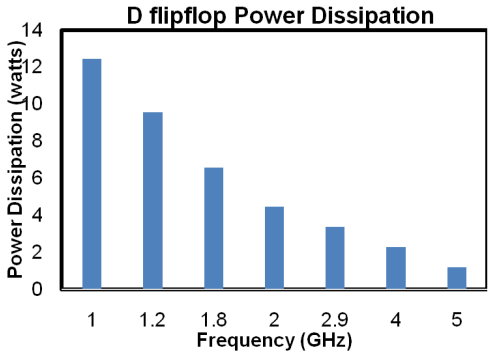

Fig. 6. Power dissipation and Frequency graph of D Flip Flop.

V. CONCLUSION

The frequency scaling technique using the artix7 family and ambient temperature 25℃ is used in order to design a low power memory cell. With the increase in frequency, the total power value is decreasing. At 1GHZ there is 13.4% reduction in power dissipation, similarly at 1.2GHZ the reduction in power dissipation is 11.5%, at 1.8GHZ it is 7.6%, 6.6% at 2GHZ, 4.5% at 3GHZ, for 4GHZ the reduction in power dissipation is 2.32%, at 5GHZ it is 1.17% for SR flip flop also the minimum value of total power is 0.084 at 8GHZ and maximum value of total power is 0.097 at 1GHZ. In case of D flip flop, at 1GHZ there is 12.5% reduction in power dissipation, at 1.2GHZ there is 9.6% reduction in power dissipation, similarly 6.6% at 1.8GHZ, 4.49% reduction in power dissipation at 2GHZ, 3.4% at 2.9GHZ, 2.3% reduction at 4GHZ and 1.19% at 5GHZ also the minimum value of total power is 0.084 at 8GHZ and maximum value of total power is 0.096 at 1GHZ.The leakage power in both the cases is 0.082.

VI. FUTURE SCOPE

Dealing with power consumption is quickly becoming one of the most challenging issues in digital system design. This optimization should be done at all levels of the design hierarchy including the technology, layout, circuit, architectural, logic and arithmetic levels.

Conflict of Interest. There is no conflict of interest for this research work.

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